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Asynchronous Down counter

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module Asy\_Co (

input wire clk, // clock input

input wire rst, // synchronous reset

output reg [2:0] q // 3-bit counter output

);

initial begin

q <= 3'b0000;

end

always @(posedge clk)

begin

q <= 3'b000;

if (rst)

q <= 3'b000; // reset counter to 0

else

q <= q - 1; // increment counter

end

endmodule